WHAT IS CLAIMED IS:

1. A multi-bit test circuit for determining a match in logical level among a plurality of data bits read out in parallel from a memory array, comprising:

a plurality of first determining circuits, arranged corresponding to said plurality of data bits, each for receiving, as a pair, a corresponding data bit and a teacher data bit placed in a predetermined relation with said corresponding data bit in the plurality of data bits, and determining a match in logical level between received data bits, data bits in each pair including different teacher data bits from other pair(s); and

a final determining circuit for outputting a final determination signal indicating a match in logical level among said plurality of data bits in accordance with output signals of said plurality of first determining circuits.

2. The multi-bit test circuit according to claim 1, wherein

said plurality of data bits are divided into a plurality of groups each having a predetermined number of data bits, and

each of said plurality of first determining circuits receives, as a teacher data bit thereof, a data bit in a different group from a corresponding group including a corresponding data bit and in a same position in the different group as a position of the corresponding data bit in the corresponding group.

3. The multi-bit test circuit according to claim 1, wherein

said plurality of data bits are applied in parallel, and divided into a plurality of groups each having a same data width, and

each of said plurality of first determining circuits receives, as said teacher data bit, a data bit that is in a group adjacent to a corresponding group including a corresponding data bit and in a corresponding position in the adjacent group to a position of the corresponding data bit in the corresponding group.

4. The multi-bit test circuit according to claim 3, wherein said plurality of first determining circuits is smaller in number than said plurality of data bits.

5. The multi-bit test circuit according to claim 3, wherein each of said plurality of first determining circuits receives, as said teacher data bit, a data bit in a corresponding position, to a position of a corresponding data bit, in a group adjacent in cyclic manner among said plurality of groups.

6. The multi-bit test circuit according to claim 1, wherein said plurality of data bits are applied in parallel, and divided into a plurality of groups having a same bit width; and

said plurality of first determining circuits are arranged corresponding to said plurality of data bits, respectively, and receive, as teacher data bits, data bits in corresponding positions, in groups different from the groups of corresponding data bits.

7. The multi-bit test circuit according to claim 1, wherein said plurality of data bits are applied in parallel, and are divided into a plurality of groups of a same bit width, and

said plurality of first determination circuits comprise a plurality of gate circuits, arranged corresponding to respective data bits of a predetermined number of groups of said plurality of groups, each for receiving a corresponding data bit and a data bit located in a corresponding position in a different group from a corresponding group including the corresponding data as the teacher data bit and determining a match in logic level between the corresponding data bit and the received teacher data bit.

8. The multi-bit test circuit according to claim 1, further comprising a teacher signal transmission bus for transmitting expected value teacher data of plural bits, wherein

said plurality of data bits are applied in parallel, and divided into a

plurality of groups each having a predetermined number of data bits; and

said teacher signal transmission bus has a same bit width as the groups of the data bits, and

said plurality of first determining circuits comprises:

a plurality of first determination gates, arranged corresponding to respective data bits in a predetermined number of groups of said plurality of groups of data bits, each receiving a corresponding data bit and a data bit in a corresponding position in a group different from a group including the corresponding data bit as said teacher data bits; and

a plurality of second determination gates, arranged corresponding to the respective data bits in other groups, each receiving a corresponding data bit in a corresponding group and a corresponding expected value teacher data bit of said expected value teacher data of plural bits.

9. The multi-bit test circuit according to claim 1, wherein the data bits each are coupled to a same number of first determining circuits of said plurality of first determination circuits.

10. The multi-bit test circuit according to claim 1, wherein an interconnection layout of each data bit to a corresponding first determining circuit is so set that interconnection loads of all the data bits are substantially the same with each other.

11. A multi-bit test circuit comprising:

a plurality of data lines for selecting plurality of data bits, said plurality of data bits being divided into at least three groups having a same bit width;

a plurality of determination gates, arranged corresponding to said plurality of data lines, each receiving, as teacher data, a data bit in a different group from a corresponding group and determining a match in logical level between a data bit of a corresponding data line and received teacher data; and

a final determination circuit for generating a signal indicating a

match in logical level among said plurality of data bits in accordance with output signals of said plurality of determination gates.

12. The multi-bit test circuit according to claim 11, wherein said teacher data is located in a same position in the different group as a position of the corresponding data bit in the corresponding group.